IN THE CLAIMS

Please amend the claims as follows:

1. (Original) A semiconductor device comprising:

a first discontinuous active region in which only a gate of a pMISFET is placed;

a first continuous active region in which gates of three or more respective pMISFETs are arranged; and

a trench isolation surrounding the first discontinuous active region and the first continuous active region,

wherein gates of pMISFETs of a first type are arranged in the first continuous active region, whereas a gate of a pMISFET of a second type, which needs higher current driving capability than the pMISFETs of the first type, is placed in the first discontinuous active region.

2. (Currently amended) The semiconductor device of claim 1, including a two-input active region which is surrounded by the trench isolation and in which gates of two respective pMISFETs are disposed,

wherein gates of two respective pMISFETs of ~~the second type~~ a third type, which need higher current driving capability than the pMISFETs of the first type, are disposed in the two-input active region.

3. (Withdrawn) The semiconductor device of claim 2, wherein a dummy gate for separation is provided between the gates of the two pMISFETs of the third ~~second~~ type.

4. (Withdrawn) The semiconductor device of claim 1, wherein the first discontinuous active region is designed to have a width in the range greater than or equal to five times the gate length and less than or equal to 8.5 times the gate length, in the gate length direction.

5. (Withdrawn) The semiconductor device of claim 1, wherein the first discontinuous active region is designed to have a width in the range greater than or equal to 0.6 μm and less than or equal to 1.0 μm in the gate length direction.

6. (Currently amended) The semiconductor device of claim 1, including:

a second discontinuous active region which is surrounded by the trench isolation and in which only a gate of an nMISFET is placed; and

a second continuous active region which is surrounded by the trench isolation and in which gates of three or more respective nMISFETs are arranged,

wherein gates of nMISFETs of the first type are arranged in the second discontinuous ~~continuous~~ active region, whereas a gate of an nMISFET of the second type, which needs higher current driving capability than the nMISFETs of the first type, is placed in the second continuous ~~discontinuous~~ active region.

7. (Currently amended) A semiconductor device comprising:

a discontinuous active region in which only a gate of an nMISFET is placed;

a continuous active region in which gates of three or more respective nMISFETs are arranged; and

a trench isolation surrounding the discontinuous active region and the continuous active region,

wherein gates of nMISFETs of a first type are arranged in the discontinuous ~~continuous~~ active region, whereas a gate of an nMISFET of a second type, which needs higher current driving capability than the nMISFETs of the first type, is placed in the continuous ~~discontinuous~~ active region.

8. (Currently amended) The semiconductor device of claim 7, including a two-input active region which is surrounded by the trench isolation and in which gates of two respective nMISFETs are disposed,

wherein gates of nMISFETs of a third type, which need higher current driving capability than the nMISFETs of the second type, ~~the first type~~ are disposed in the two-input active region.

9. (Withdrawn) The semiconductor device of claim 7, including a dummy gate provided between the trench isolation and one of the gates of the nMISFETs of the second type located at an end thereof in the continuous active region.

10. (Withdrawn) The semiconductor device of claim 7, wherein a distance between the trench isolation and one of the gates of the nMISFETs of the second type located at an end thereof in the continuous active region is greater than or equal to four times the gate length.

11. (Withdrawn) The semiconductor device of claim 8 [[7]], wherein a gate of an nMISFET of a fourth [[third]] type in which a drain parasitic capacitance, a channel leakage current or a gate leakage current needs to be reduced more than in the nMISFETs of the first type is placed in the discontinuous active region or the two-input active region.